REMARKS

Claims 1-22 are pending in the present application. The Examiner has rejected claims 1-22. Claims 1, 10, 14-17, and 19-21 have been amended. Reconsideration in view of the following arguments is kindly requested.

Specification

Applicants thank the Examiner for pointing out the minor discrepancy in the language of paragraphs [0003] and [0031]. In accordance, with the Examiner's suggestions, Applicants have amended a term in each of these paragraphs to correct these minor errors.

Claim Objections

Applicants thank the Examiner for pointing out the minor claim language informality in claim 1. In accordance, with the Examiner's suggestion, Applicants have amended the word which the Examiner has objected to. Withdrawal of this objection is kindly requested.

Claim Rejections – 35 U.S.C. § 112

The Examiner has rejected claims 10-11 under 35 U.S.C. § 112, second paragraph, as being indefinite for a lack of antecedent basis. Accordingly, Applicants have amended claim 10, thereby alleviating any outstanding antecedent basis concerns. Withdrawal of this rejection is kindly requested.

Claim Rejections – 35 U.S.C. § 102

The Examiner has objected to claims 14-17 under 35 U.S.C. § 102(b) as being anticipated by Garrett, Sr. et al., USP 4,285,433. This rejection is respectfully traversed.

Applicants submit that Garrett fails to teach or disclose a tape displacement device which separates a protective tape portion from a protected surface of an individual chip, while the individual chip is attached to a chip pad, as recited in claim 14.

Garrett discloses removing semiconductor dice 16, from a severed wafer 10 by using a vacuum pickup 47 to remove the dice 16, once adhesive tape layers 12 and 14 have been removed from the dice 16. See Fig. 2 of Garrett. Applicants submit that removing these adhesive layers from the dice 16 also includes removing the actual dice 16 away from the adhesive tape layers. For instance, Garrett discloses another tape layer 18 which is advanced to cause a forward advancing edge 46 of the dice 16 along a row 36 to pull away from tape layer 12 and pass across slot 38 while adhesive tape layers 12 and 14 remain attached to tape layer 18. See col. 4, lines 39-43. Garrett does not disclose removing a protective tape portion from a protected surface of an individual chip while the individual chip is attached to a chip pad, as recited in claim 14.

Accordingly, Applicant submits that claim 14 and those claims dependent thereon are allowable over the prior art. Withdrawal of this rejection is kindly requested.

Claims 19-21 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Farnworth et al., USP 6,202,292. This rejection is respectfully traversed.

Applicants submit that Farnworth fails to teach or disclose a tape removal device for removing a protective tape portion from a protected surface of an individual chip, while the individual chip is attached to a chip pad, as recited in claim 19.

Farnworth discloses removing a carrier film from a semiconductor die by actuating a cap to contact the die and push the die away from the carrier film while a vacuum positioned above the die pulls the die away from the film. See col. 2, lines 9-14 of Farnworth. Applicants submit that Farnworth fails to teach or disclose removing a protective tape portion from a protected surface of an individual chip, while the individual chip is attached to a chip pad.

Accordingly, Applicant submits that claim 19 and those claims dependent thereon are allowable over the prior art. Withdrawal of this rejection is respectfully requested.

Claims 1-3, 5-6 and 8-22 are rejected under 35 U.S.C. § 102(e) as being anticipated by Kawakami, USP 2003/0190795. This rejection is respectfully traversed.

Applicant has perfected the priority of the present application, which antedates Kawakami, by providing an English translation of the Korean counterpart patent application which was filed on December 23, 2002 prior to the filing date of Kawakami.

Accordingly, Applicant submits that Kawakami is not valid prior art under 35 U.S.C. § 102. Withdrawal of this rejection is kindly requested.

Claim Rejections – 35 U.S.C. § 103

Claims 1-6, 8-11 and 13 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamada et al., USP 6,297,131 in view of Huang et al., USP 6,650,006. This rejection is respectfully traversed.

Applicant submits that the Examiner has failed to establish a *prima facie* case of obviousness when rejecting claim 1, for at least the reason that there is no evidence that the teachings of Yamada and Huang would be obvious to combine.

Yamada discloses a method for grinding and dicing a wafer, which includes applying a protective tape 32 to a wafer 30 and mounting the wafer on a dicer tape 36. See col. 5, lines 46-50. After the wafer 30 is grinded, it may be diced and the wafer may be removed from the protective tape 32. See col. 7, lines 33-36. The wafer 30 may be diced into individual semiconductor chips 30a which may be separated from the protective tape 32 by applying a vacuum pickup 44.

Applicants agree with the Examiner that Yamada fails to teach or disclose attaching an individual chip to a chip pad as recited in claim 1, however, Applicants disagree that the stacked chip package disclosed in Huang would be obvious to combine with the manufacturing method disclosed in Yamada.

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). See MPEP § 2143 - § 2143.03 for decisions pertinent to each of these criteria.

Applicants submit that the teachings of Yamada and Huang, although related to semiconductor devices, do not suggest or provide any motivation for combining one with the other. For instance, the method for grinding a semiconductor wafer disclosed in Yamada, refers only to mounting the wafer on a protective tape before grinding the backside of the wafer and dicing the wafer into individual dice. While Huang, discloses forming a stacked chip configuration by holding a chip firmly during a wire bonding procedure without the need for supporting elements, thus several chips may be mounted on top of each other without affecting the electrical connections of the chips to a chip carrier. Applicants submit that the method of mounting chips disclosed in Huang does not provide any motivation or suggestion for combining the chip manufacturing process disclosed in Yamada.

Applicants respectfully remind the Examiner that the initial burden is on the examiner to provide some suggestion of the desirability of doing what the inventor has done. "To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a

convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." Ex parte Clapp, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985). See MPEP § 2144 - § 2144.09 for examples of reasoning supporting obviousness rejections. Applicants submit that the Examiner has provided no evidence of a suggestion or desirability for combining Yamada and Huang to reject claim 1.

Accordingly, Applicants submit that claim 1 and those claims dependent thereon are allowable over the prior art. Withdrawal of this rejection is kindly requested.

Claim 7 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamada and Hwang and further in view of Oka, USP 2002/0048904. This rejection is respectfully traversed. Applicants submits that at least for the reasons as stated above with regard to claim 1, that claim 7 is also allowable over the prior art. After a cursory review of the additional reference cited Oka, Applicant submits that Oka fails to provide any further support for teaching the claim limitations of claim 7, or to render claim 7 as obvious.

Accordingly, Applicant submits that, for at least the reasons stated above, claim 7 is allowable over the prior art. Withdrawal of this rejection is kindly requested.

CONCLUSION

Accordingly, in view of the above amendments and remarks, reconsideration of the objections and rejections and allowance of each of claims 1-22 in connection with the present application is earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact John A. Castellano at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY, & PIERCE, P.L.C.

By _____
John A. Castellano, Reg. No. 35,094

P.O. Box 8910
Reston, Virginia 20195
(703) 668-8000

JAC/KE:js

Attachment: Verified English Translation of Korean Patent Appl. No. 02-82672